REMARKS

Reconsideration of the above-identified application in view of the following remarks is respectfully requested.

A. Claim Status / Explanation of Amendments

Applicants note that the Office Action Summary lists claims 1-8 as pending. However, Applicants would like to point out that claims 7 and 8 were canceled in the July 26, 2007 amendment.

Claims 1-6 are pending and were rejected pursuant to 35 U.S.C. § 103(a) as allegedly being unpatentable over Japanese Patent Application No. 09-323292 to Mitsuru, et al. ("Mitsuru") in view of Japanese Patent Application No. 2001-224740 to Hieda ("Hieda") and further in view of U.S. Patent No. 6,975,018 B2 to Ohmi, et al. ("Ohmi") and still further in view of U.S. Patent Application No. 2001/0043085 A1 to Shimazaki, et al. ("Shimazaki"). [10/22/07 Office Action, p. 2].

B. Claims 1-6 are Patentable over the Cited References

The rejection of claims 1-6 as allegedly being obvious over Mitsuru in view of Hieda and further in view of Ohmi and still further in view of Shimazaki is respectfully traversed. As set forth in detail below, each of the cited references, whether alone or in combination, fail to teach, disclose, or suggest each and every element of these claims. [MPEP 2143.03]. Accordingly, the Section 103 rejection should be withdrawn.

Applicants' claim 1 recites:

> 1. A switched capacitor circuit formed on a substrate of a semiconductor integrated circuit, comprising:
>
> a switch formed by connecting in parallel a p-channel MIS field-effect transistor with an n-channel MIS field-effect transistor in

> which a projecting portion is formed by a silicon substrate having a first crystal surface as a primary surface and a second crystal surface as a side surface, terminated hydrogen on the silicon surface is removed in a plasma atmosphere of an inert gas, then a gate insulating film is formed on at least a part of the top surface and the side surface of the projecting portion at a temperature at or lower than about 550°C in the plasma atmosphere, a gate is formed on the gate insulating film, and a drain and a source are formed on both sides enclosing the gate insulating film of the projecting portion; and a capacitor,
>
> wherein gate widths of a top surface and a side surface of the p-channel MIS field-effect transistor and the n-channel MIS field-effect transistor are set such that the current drive capability of the p-channel MIS field-effect transistor can be substantially equal to current drive capability of the n-channel MIS field-effect transistor.

At the outset, the Office Action recognizes that Mitsuru as modified by Heida and Ohmi does not recite the limitation wherein the "gate widths of a top surface and a side surface of the p-channel ... and the n-channel [metal insulator semiconductor] MIS field-effect transistor are set such that the current drive capability of the p-channel ... can be substantially equal to current drive capability of the n-channel MIS field-effect transistor" as recited in Applicants' pending claim 1. [10/22/07 Office Action, p. 6]. In attempting to overcome this deficiency the Office Action relies on Shimazaki which is directed, *inter alia*, to a semiconductor integrated circuit realizing high-speed and low-power operation. [Shimazaki, ¶0001]. In supporting this contention, the Office Action refers to ¶0128 of Shimazaki, the relevant portion of which states:

> It is said that the subthreshold leak of a MOS transistor is proportional to the gate width of the MOS transistor. Usually, in a CMOS circuit, the gate width of the pMOS transistor having weaker driving force is set to be wider than that of the nMOS transistor. It is considered that the subthreshold leak of the pMOS transistor is larger than the other. [Shimazaki, ¶0128].

Based on the above, the Office Action contends that Shimazaki provides the requisite teaching, suggestion, or motivation for a person of ordinary skill in the art to conceptualize the gate width and structure of Applicants' n- and p-channel MIS field-effect transistors.

Applicants respectfully disagree and note that conventional semiconductor integrated circuits are constructed from electronic devices formed within the surface plane of the substrate (e.g., the Si(001) surface). Thus, desired changes in device performance are traditionally obtained by adjusting the dimensions (i.e., the gate width and length) within the two-dimensional plane of the surface. While Shimazaki discloses setting the gate width of a pMOS transistor larger than that of a nMOS transistor, there is provided absolutely no teaching, suggestion, or motivation for accomplishing this by projecting the gate vertically, into a third dimension such that there is a "projecting portion" comprising a "first crystal surface as a primary surface and a second crystal surface as a side surface" as recited in Applicants' claim 1.

Moreover, Applicants note that none of the cited references disclose using differing "projection portion" heights in order to obtain the different gate widths necessary to equate the current drive capabilities of the n- and p-channel MIS transistors. In Heida, for example, only a single height for the 'fence' (13) is illustrated in each of the drawings provided. Thus, Applicants respectfully assert that not only do the cited references fail to teach or suggest all the claim limitations, but there also is provided absolutely no suggestion or motivation for combining their teachings in order to conceptualize Applicants' switched capacitor circuit. As such, the basic criteria for establishing a *prima facie* case of obviousness has not been met and the obviousness rejection should therefore be withdrawn. [MPEP 2143].

Accordingly, Mitsuru, Heida, Ohmi, and Shimazaki - whether alone or in combination - fail to teach, disclose or suggest a switched capacitor circuit comprised of a "projecting portion

[which] is formed by a silicon substrate having a first crystal surface as a primary surface and a second crystal surface as a side surface" wherein the "gate widths of a top surface and a side surface of the p-channel MIS field-effect transistor and the n-channel MIS field-effect transistor are set such that the current drive capability of the p-channel MIS field-effect transistor can be substantially equal to current drive capability of the n-channel MIS field-effect transistor" as recited in Applicants' pending claim 1. Applicants respectfully submit that claim 1 is patentably distinct from Mitsuru, Heida, Ohmi, and Shimazaki for at least this reason. Claim 6 is directed to a semiconductor integrated circuit comprising the switched capacitor circuit of claim 1 and, as such, is asserted to be patentably distinct for at least similar reasons. Claims 2-5 depend from claim 1 and are asserted to be in condition for allowance for at least similar reasons. The Section 103 rejection should therefore be withdrawn. Applicants respectfully submit that all of the pending claims are now allowable for the above reasons and early, favorable action in that regard is requested.

Applicants have chosen in the interest of expediting prosecution of this patent application to distinguish the cited documents from the pending claims as set forth above. These statements should not be regarded in any way as admissions that the cited documents are, in fact, prior art. Finally, Applicants have not specifically addressed the rejections of the dependent claims. Applicants respectfully submit that the independent claims, from which they depend, are in condition for allowance as set forth above. Accordingly, the dependent claims also are in condition for allowance. Applicants, however, reserve the right to address such rejections of the dependent claims in the future as appropriate.

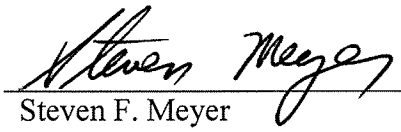
CONCLUSION

For the above-stated reasons, this application is respectfully asserted to be in condition for allowance. An early and favorable examination on the merits is earnestly solicited. In the event that a telephone conference would facilitate the examination of this application in any way, the Examiner is invited to contact the undersigned at the number provided.

THE COMMISSIONER IS HEREBY AUTHORIZED TO CHARGE ANY ADDITIONAL FEES WHICH MAY BE REQUIRED FOR THE TIMELY CONSIDERATION OF THIS AMENDMENT UNDER 37 C.F.R. §§ 1.16 AND 1.17, OR CREDIT ANY OVERPAYMENT TO DEPOSIT ACCOUNT NO. 13-4500, ORDER NO. 5000-5295.

Respectfully submitted,
MORGAN & FINNEGAN, L.L.P.

Dated: December 26, 2007

By: 
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